WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a substrate;

a first interlayer dielectric located on the substrate;

a connection node located in the first interlayer dielectric in a first region;

a second interlayer dielectric located on the first interlayer dielectric;

an integrated capacitor having a top electrode and a bottom electrode formed in the second interlayer dielectric such that the bottom electrode is in electrical contact with the connection node; and

a connection node contact positioned through the second interlayer dielectric providing an electrical connection to the connection node.

2. The semiconductor device of claim 1, wherein a DRAM cell is located in a second region of the substrate.

3. The semiconductor device of claim 2, wherein the DRAM cell comprises a transistor located on the substrate and a storage capacitor positioned in the second interlayer dielectric.

4. The semiconductor device of claim 3, wherein a bottom electrode of the storage capacitor is in electrical contact with a source/drain region of the transistor.

5. The semiconductor device of claim 4, wherein the connection node and a device contact in the first interlayer dielectric are made of a first material, the device contact electrically

connecting the bottom electrode of the storage capacitor and the source/drain region of the transistor.

6. The semiconductor device of claim 5, wherein the first material is a material selected from the group consisting of a metal, an elemental metal, a transition metal, and a combination thereof.

7. The semiconductor device of claim 3, wherein the connection node and a gate of the transistor are made of a first material.

8. The semiconductor device of claim 7, wherein the first material is polysilicon.

9. The semiconductor device of claim 1, wherein the bottom electrode of the integrated capacitor is in electrical contact with the connection node via a second connection node contact.

10. A semiconductor device comprising:

a connection node located on a substrate in a first region;

a first interlayer dielectric located on the connection node;

a second interlayer dielectric located on the first interlayer dielectric;

an integrated capacitor having a top electrode and a bottom electrode formed in the second interlayer dielectric;

a first connection node contact formed through the first interlayer dielectric electrically coupling the bottom electrode to the connection node; and

a second connection node contact formed through the first interlayer dielectric providing an electrical connection to the connection node.

11. The semiconductor device of claim 10, wherein a first device is located on a second region of the substrate.

12. The semiconductor device of claim 11, wherein a first device is a DRAM cell.

13. The semiconductor device of claim 12, wherein the DRAM cell comprises a transistor located on the substrate and a storage capacitor located in the second interlayer dielectric.

14. The semiconductor device of claim 13, wherein a bottom electrode of the storage capacitor is in electrical contact with a source/drain region of the transistor.

15. The semiconductor device of claim 13, wherein the connection node and a gate of the transistor are made of a first material.

16. The semiconductor device of claim 15, wherein the first material is polysilicon.

17. The semiconductor device of claim 11, wherein the first device is a logic device.

18. The semiconductor device of claim 17, wherein the logic device comprises a transistor located on the substrate.

19. The semiconductor device of claim 18, wherein the connection node and a gate of the transistor are made of a first material.

20. The semiconductor device of claim 19, wherein the first material is polysilicon.

21. The semiconductor device of claim 18, further comprising a transistor contact positioned through the first interlayer dielectric providing an electrical connection to the transistor.

22. The semiconductor device of claim 21, wherein the first connection node contact and the transistor contact are formed of a material selected from the group consisting of a metal, an elemental metal, a transition metal, and a combination thereof.

23. The semiconductor device of claim 21, wherein the first connection node contact and the transistor contact include a barrier layer.

24. The semiconductor device of claim 23, wherein the barrier layer is formed of a material selected from the group consisting of titanium, titanium nitride, and combinations thereof.

25. The semiconductor device of claim 10, wherein a surface of the connection node is silicided.

26. A method of forming a semiconductor device, the method comprising:

providing a substrate;

forming a first interlayer dielectric on the substrate;

forming a connection node located in the first interlayer dielectric in a first region;

forming a second interlayer dielectric on the first interlayer dielectric;

forming an integrated capacitor having a first top electrode and a first bottom electrode formed in the second interlayer dielectric such that the first bottom electrode is in electrical contact with the connection node; and

forming a connection node contact through the second interlayer dielectric providing an electrical connection to the connection node.

27. The method of claim 26, further comprising forming a device on a second region of the substrate before forming the first interlayer dielectric.

28. The method of claim 27, wherein the device is a transistor.

29. The method of claim 28, further comprising simultaneously forming a contact in the first interlayer dielectric when the step of forming a connection node is performed, wherein the contact is electrically connected to the transistor.

30. The method of claim 29, further comprising simultaneously forming a storage capacitor in the second interlayer dielectric when the step of forming the integrated capacitor is performed, wherein the storage capacitor has a second top electrode and a second bottom electrode formed such that the second bottom electrode is in electrical contact with the transistor via the contact.

31. The method of claim 29, wherein the connection node and the contact are formed of a first material.

32. The method of claim 31, wherein the first material is a material selected from the group consisting of a metal, an elemental metal, a transition metal, and a combination thereof.

33. The method of claim 28, wherein the connection node and a gate electrode of the device are formed of a first material.

34. The method of claim 33, wherein the first material is polysilicon.

35. The method of claim 26, further comprising forming a second connection node contact electrically coupling the first bottom electrode to the connection node.

36. A method of forming a semiconductor device, the method comprising:

providing a substrate having at least one first region and one second region;

forming a transistor on the first region;

forming a first interlayer dielectric over the substrate;

forming a connection node in the first interlayer dielectric upon the second region, the connection node being a thickness substantially equivalent to the thickness of the first interlayer dielectric;

forming a second interlayer dielectric on the first interlayer dielectric;

forming an integrated capacitor in the second interlayer dielectric upon the second region and a storage capacitor in the second interlayer dielectric upon the first region, the integrated capacitor having a first bottom electrode being in electrical contact with the connection node and the storage capacitor having a second bottom electrode , the second bottom electrode being in electrical contact with the transistor; and

forming a connection node contact in the second dielectric layer, the connection node contact being in electrical contact with the connection node.

37. The method of claim 36, further comprising simultaneously forming a transistor contact in the first interlayer dielectric when the step of forming the connection node is performed, wherein the transistor contact electrically connects a source/drain of the transistor with the second bottom electrode.

38. The method of claim 37, wherein the transistor contact and the connection node are formed of a first material.

1 39. The method of claim 38, wherein the first material is a material selected from the group
2 consisting of a metal, an elemental metal, a transition metal, and a combination thereof.

1 40. The method of claim 36, wherein the connection node is formed of a material selected
2 from the group consisting of a metal, an elemental metal, a transition metal, and a combination
3 thereof.

1 41. The method of claim 36, wherein forming the connection node includes forming a barrier
2 layer on the first interlayer dielectric and forming a conductive layer on the barrier layer.

1 42. The method of claim 41, wherein the barrier layer is formed of a material selected from
2 the group consisting of titanium, titanium nitride, and combinations thereof.

1 43. The method of claim 41, wherein the conductive layer comprises tungsten.

44. A method of forming a semiconductor device, the method comprising:

providing a substrate having at least one first region and at least one second region;

forming a transistor on the first region and a conductive layer on the second region ;

forming a first interlayer dielectric located on the substrate and covering the transistor and the conductive layer;

forming a first connection node contact to the conductive layer through the first interlayer dielectric;

forming a second interlayer dielectric on the first interlayer dielectric; and

forming a capacitor in the second interlayer dielectric, the capacitor having a first bottom electrode and a first top electrode, the first bottom electrode being in electrical contact with the first connection node contact.

45. The method of claim 44, wherein the conductive layer is polysilicon.

46. The method of claim 44, further comprising simultaneously forming a transistor contact in the first interlayer dielectric when the step of forming the first connection node contact is performed, wherein the transistor contact electrically connects to the transistor through the first interlayer dielectric.

47. The method of claim 46, wherein the first connection node contact and the transistor contact are formed of the same material.

48. The method of claim 47, wherein the first connection node contact and the transistor contact are formed of a material selected from the group consisting of a metal, an elemental metal, a transition metal, and a combination thereof.

1 49. The method of claim 44, wherein forming the first connection node contact includes
2 forming a barrier layer on the first interlayer dielectric and forming a conductive liner on the
3 barrier layer.

1 50. The method of claim 49, wherein the barrier layer is formed of a material selected from
2 the group consisting essentially of titanium, titanium nitride, and combinations thereof.

1 51. The method of claim 49, wherein the conductive liner comprises tungsten.

1 52. The method of claim 44, wherein a surface of the conductive layer is silicided.

53. A semiconductor device comprising:

a transistor and a connection node located on the substrate;

a first interlayer dielectric blanketed on the substrate covering the transistor and the connection node;

a second interlayer dielectric blanketed on the first interlayer dielectric;

an integrated capacitor having a first top electrode and a first bottom electrode located in the second interlayer dielectric;

a storage capacitor having a second top electrode and a second bottom electrode located in the second interlayer dielectric;

a first connection node contact located through the first interlayer dielectric electrically coupling the first bottom electrode to the connection node;

a second connection node contact formed through the first interlayer dielectric providing an electrical connection to the connection node; and

a transistor contact formed through the first interlayer dielectric electrically coupling the second bottom electrode to a source/drain region of the transistor.

54. The semiconductor device of claim 53, wherein the first connection node contact, the second connection node contact and the transistor contact are made of a material selected from the group consisting of a metal, an elemental metal, a transition metal, and a combination thereof.

55. The semiconductor device of claim 53, wherein the first connection node contact, the second connection node contact and the transistor contact include a barrier layer.

56. The semiconductor device of claim 55, wherein the barrier layer is made of a material selected from the group consisting of titanium, titanium nitride, and combinations thereof.

57. The semiconductor device of claim 55, wherein the surface of the first and second connection contact node is silicided.